

## ML12052 1.1 GHz Super Low Power Dual Modulus Prescaler

# MECL PLL COMPONENTS ÷64/65, ÷128/129 DUAL MODULUS PRESCALER SEMICONDUCTOR TECHNICAL DATA

Legacy Device: Motorola MC12052A

The ML12052 is a super low power dual modulus prescaler used in phase–locked loop applications with low power dissipation of 2.7 mW at a minimum supply voltage of 2.7 V.

The ML12052 can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx or Lansdale's ML145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- The ML12052 is Pin and Functionally Compatible with the Motorola or ON Semiconductor MC12022
- Low Power 1.0 mA Typical
- 2.0 mA Maximum,  $V_{CC} = 2.7$  to 5.5 Vdc
- Short Setup Time (t<sub>set</sub>) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc
- Operating Temperature Range  $T_A = -40$  to  $85^{\circ}C$

#### **FUNCTIONAL TABLE**

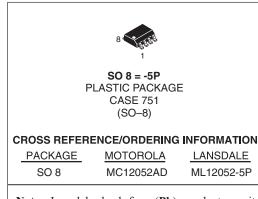
sw	МС	Divide Ratio			
Н	Н	64			
Н	L	65			
L	Н	128			
L	L	129			

NOTES: 1. SW: H = V<sub>CC</sub>, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.

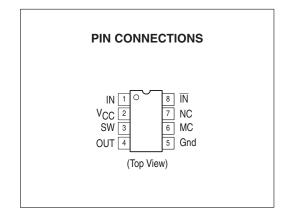
2. MC: H = 2.0 V to V<sub>CC</sub>, L = GND to 0.8 V.

#### **MAXIMUM RATINGS**

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	VCC	-0.5 to 7.0	Vdc
Operating Temperature Range	TA	-40 to 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Modulus Control Input, Pin 6	MC	-0.5 to 6.5	Vdc



**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7 \text{ to } 5.5 \text{ VDC}$ ,  $T_A = -40 \text{ to } 85^{\circ}\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave Input)	ft	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	Icc	-	1.0	2.0	mA
Modulus Control Input High (MC)	V <sub>IH1</sub>	2.0	-	V <sub>CC</sub> + 0.5 V	V
Modulus Control Input Low (MC)	V <sub>IL1</sub>	Gnd	-	0.8	V
Divide Ratio Control Input High (SW)	V <sub>IH2</sub>	V <sub>CC</sub> – 0.5 V	V <sub>CC</sub>	V <sub>CC</sub> + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V <sub>IL2</sub>	Open	Open	Open	-
Output Voltage Swing (Note 2) (C <sub>L</sub> = 8.0 pF, R <sub>L</sub> = 3.3 k $\Omega$ )	V <sub>out</sub>	0.8	1.1	-	VPP
Modulus Setup Time MC to Out @ 1100 MHz	t <sub>set</sub>	-	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	Vin	100 400	-	1000 1000	mVpp
Output Current (Note 1) $V_{CC}=2.7 \text{ V, } C_L=8.0 \text{ pF, } R_L=3.3 \text{ k}\Omega$ $V_{CC}=5.0 \text{ V, } C_L=8.0 \text{ pF, } R_L=7.2 \text{ k}\Omega$	IO	_ _	0.5 0.5	3.0 3.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 1.1 GHz

Figure 1. Logic Diagram (ML12052)

Prop. Delay

MC Setup

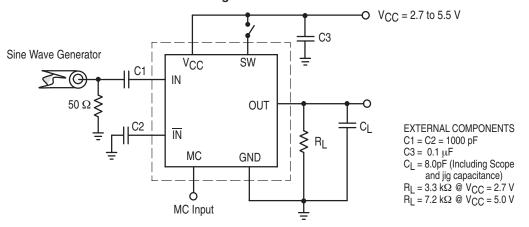
MC Release

Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

QB QB СМ D Q D QB Q QB D QB D Е G QB QB

Figure 3. AC Test Circuit



<sup>2.</sup> Valid over voltage range 2.7 to 5.5 V; R<sub>L</sub> = 3.3 k $\Omega$  @ V<sub>CC</sub> = 2.7 V; R<sub>L</sub> = 7.2 k $\Omega$  @ V<sub>CC</sub> = 5.0 V

300 200 100 MHz 0 -100 -200 -300 OHMS -400 -500 -600 -700 -800 -900 -1000 -1100 -1200 100 200 400 500 600 700 800 1000 1100 1200 300

Figure 4. Typical Input Impedance versus Input Frequency

Frequency (MHz)

Figure 5.. Generic block diagram showing prescaler connection to PLL device

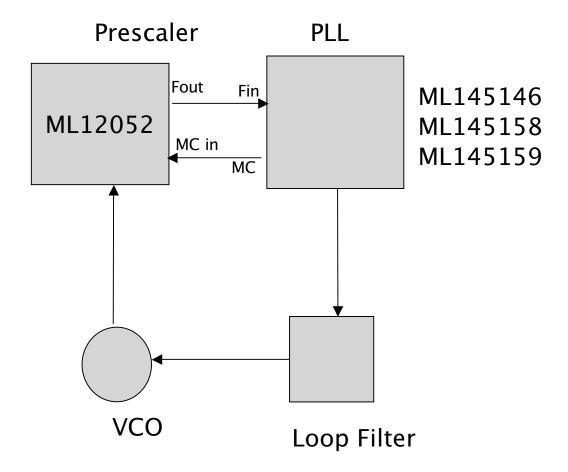
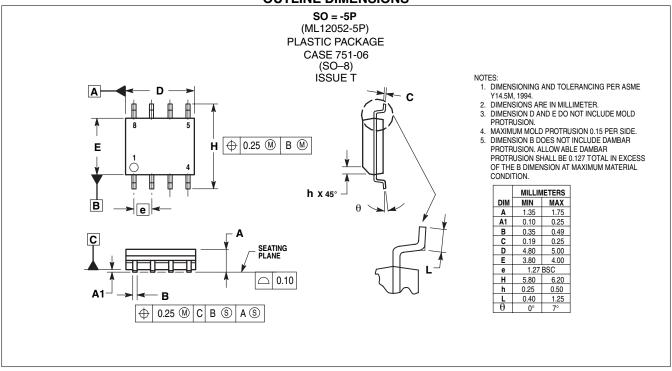


Figure 5 shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 decribes using a two-modulus prescaler technique. By using prescaler higher frequencies can be achieve than by a single CMOS PLL device.

### **OUTLINE DIMENSIONS**



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